A Non-Coherent DPSK Data Receiver With Interference Cancellation for Dual-Band Transcutaneous Telemetries

Mingcui Zhou, Mehmet Rasit Yuce, and Wentai Liu, *Senior Member, IEEE*

Abstract—A dual-band telemetry, which has different carrier frequencies for power and data signals, is used to maximize both power transfer efficiency and data rate for transcutaneous implants. However, in such a system, the power signal interferes with the data transmission due to the multiple magnetic couplings paths within the inductive coils. Since the power level of the transmitted power signal is significantly larger than that of the data signal, it usually requires a high-order filter to suppress the interference. This paper presents a non-coherent DPSK receiver without a high-order filter that is robust to the interference caused by the power carrier signal. The proposed scheme uses differential demodulation in the analog domain to cancel the interference signal for a dual-band configuration. The data demodulation also uses subsampling to avoid carrier synchronization circuits such as PLLs. The experimental results show that the demodulator can recover 1 and 2 Mb/s data rates at a 20 MHz carrier frequency, and it is able to cancel an interference signal that is 12 dB larger than the data signal without using complex filters. The demodulator is fabricated in a 0.35 μm CMOS process, with a power consumption of 6.2 mW and an active die area of $2.6 \times 1.7 \text{ mm}^2$.

Index Terms—Bandpass sampling, data telemetry, differential phase shift keying (DPSK), dual-band, inductive coupling, interference cancellation, neural implants, non-coherent, subsampling, transcutaneous.

I. INTRODUCTION

TRANSCUTANEOUS neural implants usually require wireless power for implant operation and wireless data transfer for communication. Most existing biomedical telemetries transfer both power and data using a single-band approach, in which the wireless data is modulated on the power carrier and sent through inductive coupling [1]–[4]. Furthermore, the power transmitter uses a nonlinear power amplifier to increase the power transfer efficiency [2], [3], reducing heat in the external devices and maintaining a reasonable battery lifetime.

For applications such as retinal prostheses, or brain-machine interface, it usually requires a high speed data link from the external devices to the implants to improve their functions, i.e., to increase the number of stimulation electrodes. In a single-band approach, there are two options to increase the data rate. The first option is to reduce the quality factor (Q) of the power amplifier, but this reduces the power transfer efficiency. The second

Fig. 1. System diagram of a dual-band approach.

option is to increase the carrier frequency, which will increase the skin absorption of electromagnetic energy. So, neither of these options is desirable for high-performance future implants that require high power efficiency and a high data rate.

A dual-band approach, which separates the frequencies for power and data transfer, is not subject to the tradeoff between the data rate and power transfer efficiency [5]–[7]. Thus, our proposed system targets a dual-band approach, optimizing the power and data telemetries separately. Fig. 1 shows a diagram of our dual-band system, where the power carrier is at 1 MHz and the data carrier is at 20 MHz. The data transmitter uses a Class-E power amplifier to increase the transmitter efficiency. It is desirable to keep the frequency of transmission low enough to be able to achieve high power efficiency of the Class-E amplifier as high frequencies cause more skin absorption and is sensitive to the parasitics of the PCB board and the discrete components. However, the carrier frequency should also be high enough to have one decade spectral spacing from the 1 MHz power interference. It is also easy to assign a large bandwidth for a high data rate transmission in the system.

In Fig. 1, the two coils for power transfer and the two coils for data transfer are placed coaxially to increase magnetic coupling and reduce constraints of surgical operation. This configuration, however, causes the power signal to interfere with data transmission because of the undesired magnetic couplings between the power coils and data coils. Although a high carrier frequency could be used for the data link to alleviate the effect of the power carrier interference, it is, however, avoided in the

Manuscript received July 17, 2007; revised January 27, 2008. Current version published September 10, 2008.

M. Zou and W. Liu are with the Department of Electrical Engineering, University of California, Santa Cruz, CA 95064 USA (e-mail: mingcui.zhou@gmail.com).

M. R. Yuce is with the School of Electrical Engineering and Computer Science, University of Newcastle, Callaghan, NSW 2308, Australia.

Digital Object Identifier 10.1109/JSSC.2008.2001881

targeted applications to lower the power consumption of the implant. High frequency carrier signal requires a downconversion section (e.g., mixers, analog filters) at the receiver that consumes more power. In addition, a high frequency carrier causes higher penetration loss as mentioned above [8]. Another method is to use several orders of filtering before the demodulation circuit, but this may also require a reasonable spectral separation between the power and data frequencies [9]. Our proposed data telemetry uses a differential demodulation to cancel the interference that requires no high-order filters.

Differential phase shift keying (DPSK) is chosen as the data modulation scheme because it is a convenient scheme to cancel the interference and it theoretically requires less signal-to-noise ratio (SNR) to achieve the same bit-error rate (BER) performance compared to FSK or ASK modulated signals. Conventional PSK receivers usually use a phase-locked loop (PLL) for data demodulation, however, there are several reasons to avoid a PLL in this application. First, the data telemetry signal is strongly interfered by the power telemetry, resulting in a data signal much weaker than the power interference. For the PLL to lock the PSK signal, the interference must be suppressed by a high order filter before the demodulation. Note that the same reason also applies for other methods using a delay-locked loop (DLL) in the demodulation [10]. Second, the 1 MHz signal from the power telemetry can couple to the data telemetry through parasitics, power supply, and substrates. This frequency is near or below the corner frequency of the loop filter, corrupting the voltage-controlled oscillator (VCO) output. Third, the method using PLL is based on coherent detection that requires a phase synchronization. This usually adds additional complexity that will increase the power consumption. The most commonly used COSTAS loop, for example, requires several analog multipliers for phase detection and the VCO branch.

To overcome the above problems, DPSK demodulation uses non-coherent detection to avoid using PLLs. Furthermore, the proposed scheme can demodulate the data signal with the presence of power interference and without any additional circuits (see Section II-D).

The non-coherent detection uses bandpass sampling, also called subsampling for data demodulation [11]. One method to implement subsampling is to digitize the carrier signal before sampling (*digital implementation*) [10]. This implementation, however, is sensitive to jitter when the sampling occurs at the transition edge of the digitized carrier signal. Another approach is to sample the analog signal and process it in the digital domain [12], avoiding abrupt amplitude changes in the sampled signal. When sampling at the zero-crossing point of the signal carrier, the sampling jitter will therefore cause much less error compared to its digital counterpart. The later approach, however, requires an analog-to-digital converter (ADC) which consumes too much power for implantable devices with a high data rate. The proposed scheme solves the problem by sampling the analog signal and processing it in the analog domain itself, which requires no ADC for data demodulation. Section II will explain the data modulation and demodulation schemes. Section III will describe the circuit implementation and Section IV will show the experimental results of the demodulator and a prototype system.

II. DATA MODULATION AND DEMODULATION

A. Data Modulation

Differential PSK (DPSK) modulation encodes the binary data as the phase differences of the carrier signal. In the proposed DPSK modulation, a “1” is coded as a phase shift of 180° and a “0” is coded as no phase shift. The proposed scheme has different coding for different data rates, for the purpose of interference cancellation. When the data rate is 1 Mb/s, “1” or “0” are coded by the phase differences between two *successive* symbols. When the data rate is 2 Mb/s, the data is coded by the phase difference of symbols separated by two symbol periods (1 μ s). This coding method ensures that any two corresponding symbols are separated by one period of the interference from the power telemetry (1 μ s), so the corresponding symbols encounter the same phase interference. A detailed mechanism of interference cancellation will be explained later in Section II-D.

B. Demodulation Using Subsampling

The proposed DPSK receiver uses subsampling, in which the sampling frequency is lower than the carrier frequency. It is also called bandpass sampling as it samples the bandpass signal without down-mixing. In the proposed scheme, the relationship between the sampling frequency (f_s), the carrier frequency (f_c), and the data rate (f_d) satisfies (1) and (2). The first equation avoids the loss of phase information, i.e., not always sampling at the zero crossing points of the carrier signal. The second equation is necessary when the phase information is translated to amplitude of the sample in our design—when there is a phase shift of 180° , the samples of corresponding symbols are different; when there is no phase shift, the corresponding samples are the same. To satisfy the above two criteria, the variable a in (1) can be any non-negative integer, and the variable b in (2) can be any positive integer. When $a = 0$, the sampling frequency is two times the Nyquist rate, and it falls in the category of over-sampling. When $a > 0$, it is subsampling.

$$f_s = 4f_c/(2a + 1) \quad (a = 0, 1, 2 \dots) \quad (1)$$

$$f_s = 4b \cdot f_d \quad (b = 1, 2, 3 \dots) \quad (2)$$

In the proposed system, $a = 2$, resulting in a sampling frequency of 16 MHz for a carrier frequency of 20 MHz, and the sampling frequency is provided by a crystal oscillator. The value of $1/(2a + 1)$ is inverse proportional to the amount of out-of-band noise being aliased into the signal band. A smaller value of a corresponds to a higher sampling rate, which also has more samples of each symbol and helps to optimize the SNR using the proposed demodulation scheme (see subsection *SNR* and Appendix for details). The sampling frequency is therefore chosen as a compromise between power, area and SNR—a higher the sampling frequency will have better SNR; however, it requires more power consumption and a larger switched-capacitor array for storing sample values.

One of the targeted application for this data telemetry is retinal prostheses, whose data rate is determined by the number of electrodes, stimulation pattern, and refresh rate [7]. Assume the retinal prosthesis has 14 bits for each biphasic stimulation

Fig. 2. The proposed data demodulator in the data receiver.

pattern, 1000 electrodes, and a refresh rate of 60 Hz, the required data rate is about 0.84 Mb/s. So the targeted data rate is about 1 to 2 Mb/s for accommodating communication overhead and providing expansion flexibility. According to (2), given the sampling frequency of 16 MHz, $b = 4$ for a data rate of 1 Mb/s, and $b = 2$ for 2 Mb/s. Note that the exact data rate is chosen to be a multiple of the power transfer frequency (1 Mb/s or 2 Mb/s) for ease of canceling the interference (see Section II-D for details) [13].

When the relationship in (1) and (2) are satisfied, the data demodulation can be performed as follows. In the data receiver, a passive first-order high-pass filter (HPF) limits the power interference level, and a band-limited amplifier buffers the signal for the sampling circuits (see Fig. 2). The HPF and the band-limited amplifier, in conjunction, provide bandpass filtering for the sampling circuits. To detect a phase change, an earlier symbol is sampled and held (S/H) for one or two symbol periods before being compared to the current symbol (i.e., differential decoding). When the data rate at 1 Mb/s and the sampling frequency is 16 MHz, each symbol has 16 samples. The comparison is performed by taking the sample difference of corresponding symbols. An accumulator then sums the absolute sample differences and a bit slicer compares this accumulated value to a reference and outputs the binary data. When the accumulator output is higher than the reference voltage, it indicates a phase shift (a “1”); when the accumulator output is zero, it indicates no phase shift (a “0”). Once the bit slicer decides the data, the accumulator is reset and ready for integrating again.

C. Data Clock Synchronization

According to the demodulation method, the accumulator is reset at the symbol edge for proper operation. This reset signal is provided by the data clock whose phase is approximately aligned with the symbol edge. The data clock is divided from the 16 MHz sampling clock. When the data rate is 1 Mb/s, the data clock has 16 possible phases after frequency division. To align the data clock phase with the symbol edge, the clock phase closest to the symbol edge is searched during a preamble sequence “1, 0, 1, 0, ...”. The symbol edge is recaptured at the beginning of every data packet to compensate for the phase drift due to the crystal frequency deviation.

The method for locating the symbol edge is to reset the accumulator using different clock phases, and choose one by observing the accumulator outputs. Fig. 3 shows accumulator out-

Fig. 3. (a) Output of the accumulator when resetting at different clock phases. (b) The process of data clock synchronization. Top waveform is the differential integrator (the accumulator) outputs during the preamble sequence, and the bottom waveform is the integrator reset signal.

puts when it is reset at different phases for data pattern “1 0 1 0 ...”. In Fig. 3(a), V_x and V_y are the two consecutive accumulator outputs and the vertical gray lines indicate the symbol edges. When the accumulator is reset at the symbol edge, V_x is at its minimum and V_y is at its maximum. If the accumulator is reset before the midsymbol, $V_x < V_y$. When it is reset after the midsymbol, $V_x > V_y$. So when the reset clock phase shifts from before the midsymbol to after the midsymbol, the sign of $(V_x - V_y)$ changes. Note that V_x and V_y are exchangeable and there will always be a sign change of $(V_x - V_y)$ when the reset phase passes the midsymbol. So if the reset clock phase is shifted sequentially, the midsymbol can be located by detecting this sign change. Once the midsymbol is detected, a delay of a half symbol period is added to the midsymbol to get the symbol edge.

At the beginning for searching for the optimum clock phase, the accumulator reset is first chosen arbitrarily from 16 possible phases. The accumulator outputs are recorded for two consecutive symbol periods to get the value of V_x and V_y , and the sign of $(V_x - V_y)$ is evaluated and stored. The reset clock phase is then shifted, and new values of V_x and V_y will be obtained in the next two symbol periods. If the signs of $(V_x - V_y)$ are the same, the previous steps repeat until a sign difference is found. Fig. 3(b) shows the accumulator outputs and reset phase shifts during the preamble sequence. Note that each possible phase requires two symbol periods to obtain the sign of $(V_x - V_y)$ and 1/16th symbol period delay to shift to the next clock phase. It also requires half a symbol period delay to located the symbol

edge after the midsymbol is found. So in the worst case, 34 symbol periods are required, in which all 16 possible phases are searched before finding the clock phase closest to the symbol edge.

When the data rate is 2 Mb/s, the data clock is derived from a 16 MHz sampling clock with eight possible phases. In the worst case, the symbol edge is captured in 17 symbol periods, when all eight possible phases are searched before finding the one closest to the symbol edge.

D. Interference Cancellation

The power telemetry operates at a different, but lower frequency than the data telemetry. As the data coils are placed coaxially with the power coils, the power signal (@ 1 MHz) interferes with the data signal (@ 20 MHz). According to the proposed DPSK coding, any two compared samples are separated by a duration of 1 μ s, which corresponds to one period of the interference from the power telemetry. So any two compared samples encounter the same phase power interference— $A_{pwr} \cos(\omega_{1M}t + \theta_1)$ and $A_{pwr} \cos(\omega_{1M}t + \theta_1 + 2\pi)$. When taking samples' differences, the interference is canceled without additional filters. Furthermore, other periodic noise, such as high order harmonics generated by the power transmitter, is canceled by the same mechanism. Note that the ripple of the recovered power supply is also a periodic signal at 1 MHz, so it will affect the circuit in a periodic manner. If the effect of V_{DD} ripple is not rejected completely by the differential circuits, the residue error is then canceled by differential demodulation for the same reason as interference cancellation. However, this interference-cancellation scheme only applies for certain cases, e.g., when the data rate is a multiple of the power carrier frequency.

E. SNR

Subsampling will degrade the SNR by aliasing the out-of-band noise into the signal band, but this degradation is much less severe in the proposed scheme because the under sampling ratio (f_c/f_s) is small. Furthermore, the accumulation of the sample differences in the analog domain helps to optimize the SNR. The SNR after the integration is $m/2$ times the SNR of each sample, and m is the number of samples in one symbol period (see Appendix). Note that this SNR optimization also applies to noise induced by random sampling jitter or any other noise with of random nature. In the proposed system, when the data rate is 2 Mb/s and $m = 8$, the SNR after integration is 6 dB higher than the SNR of each sample.

F. Sampling Jitter

Jitters from non-ideal sampling clocks cause sampling error. The ratio between the sampling error over the signal level is shown in (3). The sampling error and signal amplitude are ΔS and A_{sig} respectively. ω_{20M} is the 20 MHz carrier frequency in radius, and $\Delta\tau$ is the sampling jitter. When the sampling jitter is 1 ns, it approximately translates to an equivalent SNR of 20 dB according to (3).

$$\frac{\Delta S}{A_{sig}} = \frac{|d(\sin \omega_{20M}t)\Delta\tau|}{dt} = \omega_{20M} |\cos(\omega_{20M}t)| \Delta\tau. \quad (3)$$

G. Frequency Mismatch

The frequency mismatch between the internal oscillator in the implant and the external oscillator from the transmitter site causes sampling phase drift. With the two adjacent symbols being compared, this phase drift causes a small sampling error as shown in (4). ΔE is the sampling error, A is the signal amplitude, T_d is the time difference between the two compared samples, ω is the carrier frequency, φ is the phase of the carrier at the sampling point, and $\Delta\omega$ is the frequency difference between the transmitter and receiver crystal oscillator.

$$\begin{aligned} |\Delta E| &= |A \cos[(\omega + \Delta\omega) \cdot T_d + \varphi] - A \cos(\omega \cdot T_d + \varphi)| \\ &\approx 2A \left| \sin \frac{\Delta\omega \cdot T_d}{2} \right| \cdot \left| \sin \left(\left(\omega + \frac{\Delta\omega}{2} \right) \cdot T_d + \varphi \right) \right| \quad (4) \\ \max |\Delta E| &: 2A \left| \sin \frac{\Delta\omega \cdot T_d}{2} \right| \approx A \Delta\omega \cdot T_d \\ \rightarrow \text{average} |\Delta E| &: 2A \left| \sin \frac{\Delta\omega \cdot T_d}{2} \right| \cdot \frac{1}{2\pi} \int |\sin \theta| d\theta m \\ &= 2A \left| \sin \frac{\Delta\omega \cdot T_d}{2} \right| \cdot \frac{2}{\pi} \approx \frac{2A \Delta\omega \cdot T_d}{\pi} \\ \text{where } \theta &= \left(\omega + \frac{\Delta\omega}{2} \right) T_d + \varphi. \end{aligned}$$

In the proposed system, the maximum frequency difference ($\Delta\omega$) is 12.6 k rad/s (2 kHz), i.e., a 100 ppm difference at a 20 MHz carrier frequency (ω). When the sampling occurs at the zero-crossing point of the carrier signal and $T_d = 1 \mu$ s (one symbol period @ 1 Mb/s), the sampling error is -38 dB smaller than the original signal. When the sampling occurs at any phase of the carrier, the average sampling error is 41.9 dB smaller than the original signal. Therefore, the error due to frequency deviation is negligible and no phase tracking such as PLL is required.

Note that the frequency deviation of the crystal oscillators also causes a residual interference after interference cancellation. The analysis of frequency deviation for interference is similar to (4) except that A is now the amplitude of the interference. Assuming the power signal is 9 dB larger than the data signal, this scheme can tolerate a 0.5% frequency deviation of the power interference and still keep the remaining interference 20 dB smaller than the data signal.

III. CIRCUIT IMPLEMENTATION

A. Switched-Capacitor Units

The non-coherent DPSK demodulation scheme is translated to circuit design mainly using switched-capacitor techniques. The analog demodulation includes functions such as sampling and subtraction of two compared samples; these two functions are performed in the switched-capacitor units. Fig. 4 shows the basic operation of the switched-capacitor units, which represent part of the switched-capacitor array depicted in Fig. 5(a). All the circuits for data demodulation are designed with fully differential topology for charge injection cancellation and power supply rejection. In Fig. 4(a), the schematic on the left side is identical to the one on the right side except that the switch control signals used are different. Each switched-capacitor unit consists

Fig. 4. Operation of switched-capacitor units. (a) Schematic. (b) Timing diagram.

of two branches that produce two inputs for the differential integrator. The circled part in the figure is defined as one of the branches. In Fig. 4, for example, branch I and I' belong to the same switched-capacitor unit.

The dotted and continuous lines in each branch denotes the paths of switches used for the sampling operation and the subtraction, and they are turned "on" during the pulses Ph-1(i) and Ph-2(i), respectively. Ph-1(i) and Ph-2(i) are the two phases of a non-overlapping clock [see Fig. 4(b)]. During Ph-1(i), one signal (V_1) is simultaneously sampled on four branches (dotted paths in branch I, I', II, and II'). Two are used for comparing the current samples with corresponding ones from an earlier symbol, and the other two are used for comparing with a later symbol. During Ph-2(i), switches on the continuous line in branch II, II', III and III' are turned on, where branch III and III' store the counterpart samples from an earlier symbol (V_0). When the continuous path in branch II is conducting, the capacitance of this branch deposits a charge of $-V_1 \cdot C$ to node M+; when the continuous path in branch III is conducting, the capacitance of this branch deposits a charge of $V_0 \cdot C$ to node M+. At the end of Ph-2(i), Node M+ has charge $C(V_0 - V_1)$, and its voltage is $(V_0 - V_1)/2$ as the charge is redistributed between two sampling capacitors. The same

rule applies to branch II' and III'', where node M- has charge $-C(V_0 - V_1)$ and voltage $-(V_0 - V_1)/2$ by alternating the continuous paths as that in branch II and branch III.

B. Data Recovery

The schematic of the data recovery circuit is depicted in Fig. 5(a). In the switched-capacitor array, each shadowed bar denotes a switched-capacitor branch. After the two samples are subtracted during Ph-2(i), the sign of $(V_0 - V_1)/2$ is detected using a latch comparator. To integrate the absolute value of $(V_0 - V_1)$, this "sign" signal controls the cross-coupled switches in front of an integrator. The integrator is implemented as a folded cascade amplifier with capacitive feedback. During Ph-1($i+1$), $|V_0 - V_1|$ is integrated, and a new sample is stored on other branches simultaneously. Then the above operations (comparison and integration) repeat for the next sample in the symbol. At the end of one symbol period, the differential output of the integrator is the sum of the absolute sample differences between the current symbol and an earlier symbol, and the integrator is reset at every symbol edge. Before each reset, the integrator output is compared to a reference voltage using another differential comparator, which has a common topology

Fig. 5. (a) Schematic of the data recovery circuits. (b) Integrator output with power supply fluctuation. From top to bottom, the waveforms are: power supply with 30 mVpp ripple at 1.001 MHz, integrator output without V_{DD} ripple, integrator output with V_{DD} ripple of 30 mVpp, and demodulated DPSK data with V_{DD} ripple of 30 mVpp.

as described in [14]. Then a register latches this comparator output and generates the binary data.

The simulation results of the integrator output is shown in Fig. 5(b), where the integrator outputs corresponds to data “1 0 1 0”. The recovered power supply has a periodic fluctuation at 1 MHz and peak-to-peak variation of 1.5 mV. To test the circuit behavior under the power supply fluctuation, an unsymmetrical triangular wave is added to the power supply with a amplitudes of 30 mV (Vpp). A slightly deviated frequency is used (1.001 MHz) to include the frequency deviation between external and internal oscillators. Fig. 5(b) shows that even when the V_{DD} ripple in the simulation is much higher than the measured ripple, the integrator output is not affected, proving the robustness of the design.

C. Array Management

The switched-capacitor array consists of 20 switched-capacitor units, and each unit participates in three operations: sampling, comparison (subtraction), and integration. Since these three operations happen in three different phases, they require one and a half sampling periods to complete, where each sampling period has two non-overlapping phases (Ph-1) and (Ph-2) [see Fig. 4(b)]. These two phases are derived from the

Fig. 6. Operation of the switched-capacitor array.

16 MHz sampling clock using a common topology described in [15]. Fig. 6 shows the timing arrangement of the switched-capacitor array operation. Each rectangle in the middle of the figure represents one unit in the array, and its number indicates the sequence of the unit. The arrows on the top half of the figure denote the sampling operation, and each sampling happens at

Fig. 7. Implementation of the symbol edge detector. (a) Simplified circuit of the symbol edge detection. (b) Timing diagram.

a different time in the unit it is pointing at. The arrows at the bottom half of the figure denote the operation of comparison and integration. The time of the sampling, comparing, and integrating is indicated on the left side of these arrows.

During Ph-1($i + 1$), for example, unit 20 and unit 2 are sampling. Unit 20 stores the sample for comparing it with a later sample. Unit 2 stores the sample for comparing it with an earlier sample (in unit 4) during Ph-2($i + 1$), and the same unit performs integration during Ph-1($i + 2$). During Ph-1($i + 3$), unit 2 samples a new signal, and it stores this sample for one or two symbol periods before comparing it with its counterpart of a later symbol. This array arrangement ensures that any two compared samples are stored on adjacent sampling capacitors, so the capacitor mismatch can be minimized.

When the data rate is 1 Mb/s and the sampling frequency is 16 MHz, there are 16 samples of the previous symbol stored in the switched-capacitor array. Since there are two sample periods delay for analog demodulation, it requires two additional units to buffer two extra samples of the current symbol during this delay. Furthermore, there are always two units in the array performing comparison and integration. Therefore, 20 units in total are required for the switched-capacitor array. When the data rate is 2 Mb/s, the array stores 16 samples of the two previous symbols and each symbol has 8 samples. The rest of the units operate in the same manner as that of 1 Mb/s, so it also has an array of 20 units.

D. Symbol Edge Detector

The simplified circuit of the symbol edge detector is shown in Fig. 7(a), and Fig. 7(b) shows the timing control of the circuit. V_x and V_y are the integrator outputs for two continuous symbol periods (see Fig. 3). During phase sa1 (sb1), the sampling capacitors store the value of $V_x(V_y)$. Phase sa1_d (sb1_d) in Fig. 7(a) is the delayed version of sa1 (sb1), for canceling the switch charge injection. When the comparator is enabled [see Fig. 7(b)], it detects the sign of $(V_x - V_y)$. The sign signals are stored in two following registers, and an XOR gate detects the sign change of $(V_x - V_y)$. If a sign change is not found, the integrator reset shifts by one sampling period (62.5 ns), and then the circuit repeats the previous steps. If a sign change is found, a pulse signal is generated from the XOR gate output. This pulse signal resets a DFF array, which down-converts the 16 MHz sampling frequency to the data clock frequency and set the clock phase. Note that the average value of V_x and V_y is half of the maximum integrated value (see Fig. 3). So the $(V_x + V_y)/2$ can serve as the threshold reference voltage for the bit slicer, and this voltage is obtained by closing switch “S_{avg}” in Fig. 7(a).

IV. SYSTEM PROTOTYPE AND EXPERIMENTAL RESULTS

The demodulator is fabricated in 0.35 μm CMOS process to verify the concept of demodulation. Fig. 8 shows the die photo, in which the demodulator occupies a core area of 1.7 mm

Fig. 8. Die photo.

$\times 2.6$ mm and consumes 6.2 mW of power. Fig. 9(a) shows the testing result when the input of the demodulator is generated from an arbitrary waveform generator (AWG). From top to bottom, the waveforms are the input of the demodulator, the differential outputs of the integrator, and the demodulated binary data. The data rate is at 2 Mb/s in this setup, and the DPSK signal is coded as the phase difference between symbols separated by two symbol periods. The low frequency envelope at the demodulator input signal indicates the 1 MHz interference from the power telemetry, which is 9 dB larger than the DPSK modulated signal. The maximum interference level was limited by the maximum output range of the AWG device used in this test setup. The same chip can also demodulate signals with different carrier frequencies as shown in Table I. These frequencies satisfy the relationship between the sampling frequency and the carrier frequency as defined in (1). The fabricated demodulator is tested to recover carrier frequencies up to 68 MHz.

To test the BER, the AWG is programmed to add pseudo random noise to the demodulator input. When the SNR is 23 dB, the output NRZ data is recorded for more than 10^7 bits with no error found. So the BER is lower than 10^{-7} ; however, due to the limited recording length of our logic analyzer, the exact BER is not obtained. For applications such as retinal prostheses, the receiver uses a simple parity check. If an error is found, the data packet is simply discarded because additional error correction will require more power and stimulation delay. When the targeted BER is 10^{-7} for the stimulation application, the implant loses 1 out of 10,000 packets when each data packet is 1000 bit in length. The packet loss may lead to the loss of one frame of stimulation. But considering the stimulation frame rate is usually higher than 30 Hz, the loss is tolerable as it is similar to the effect of eye blinking.

A prototype system is built to test the demodulator chip in a real situation, which includes both the data telemetry and power

Fig. 9. Chip and prototype testing. (a) Chip testing. An arbitrary waveform generator provides the input to the demodulator. From top to bottom the waveforms are: the input of the demodulator, the differential outputs of the integrator, and the recovered NRZ data. (b) Diagram of the prototype system. (c) Prototype testing. The input of the demodulator is generated from the prototype telemetry system. From top to bottom the waveforms are: the input of the demodulator, the differential outputs of the integrator, and the recovered NRZ data.

telemetry [see Fig. 9(b)]. The DPSK modulated signal is generated using a Class-E amplifier, and is transferred through inductive coupling at 1 Mb/s. The power telemetry also provides the 1 MHz data clock to the demodulator in this setup. Both the power and data coils are placed coaxially, and the transmitter and receiver coils are separated by $1 \sim 1.5$ cm. The coil inductance for the data transmitter and receiver are $1 \mu\text{H}$ and $0.5 \mu\text{H}$ respectively. The power telemetry delivers 100 mW to the power receiver, and the signal amplitude of the demodulator input ranges from 400 mVpp $\sim$ 500 mVpp. The data receiver consists of a passive first order filter (discrete), a buffer (discrete), and the data demodulator chip. Fig. 9(c) shows the experimental results of this prototype system, in which the input of the demodulator is the signal after the buffer in the receiver. The

TABLE I
CHIP SUMMARY

Process	0.35 μ m CMOS
Signal to Interference Ratio	– 12 dB
Demodulator Input Amplitude	400–500 mV _{pp}
Carrier Frequency	20, 28, 36, 44, 52, 60, 68 MHz
Data Rate	1 or 2 Mbps
Sampling Frequency	16 MHz
Active Chip Area	2.6 x 1.7 mm ²
Power Consumption	6.2 mW

interference from the power telemetry is observed to be 12 dB higher than the data signal at the input of the demodulator, and this interference is cancelled without additional filters. The distortion of 1 MHz interference is caused by harmonics in the power amplifier and power rectification in the power receiver because both power transmitter and receiver coils are coupled to the data receiver coil. But since the distortion is periodic, it is also cancelled with differential demodulation mechanism as proved by the experimental results.

V. CONCLUSION

This paper reports a non-coherent DPSK demodulation scheme with interference cancellation for dual-band transcutaneous telemetries. There are several features of the design listed as follows. First of all, it uses subsampling to avoid carrier synchronization, such as PLLs. It cancels the interference from the power telemetry by differential demodulation, and thus avoids additional filters. In addition, it demodulates in the analog domain to avoid ADC. The design is also compatible to work with different carrier frequencies, which makes it suitable for different telemetry applications. The chip is fabricated in 0.35 μ m CMOS process with an active area of 2.6 mm $\times$ 1.7 mm, and a power consumption of 6.2 mW. This demodulator is tested in a prototype system, which includes inductively-coupled data telemetry and power telemetry. The experimental results show that when the interference is up to 12 dB larger than the signal, the demodulator can still recover the data without additional filters.

APPENDIX

The analysis of SNR for the proposed scheme is derived from (5)–(9). The SNR of each sample and the accumulated SNR after the accumulator are SNR_{sample} given in (5) and SNR_{integrated} given in (6). The average signal level of each sample is V_s . σ^2 is the variance of each sample due to the presence of noise, Pm is the number of samples in one symbol period, and D is the sum of absolute amplitude differences. The amplitudes of the current sample and the sample's counterpart

from an earlier symbol are c_i and d_i , respectively. The subscript i indicates the sequence number of a sample in one symbol.

$$\text{SNR}_{\text{sample}} = \frac{P_{\text{sig}}}{P_{\text{noise}}} \propto \frac{V_s^2}{\sigma^2} \quad (5)$$

$$\text{SNR}_{\text{integrated}} = \frac{P_{\text{sig}}}{P_{\text{noise}}} \propto \frac{(mV_s)^2}{\text{var}(D)} \quad (6)$$

$$D = \sum_{i=1}^m |c_i - d_i|. \quad (7)$$

When the noise of c_i and d_i are independent, the variance of D is given in (8). By replacing $\text{var}(D)$ in (6) with (8), the relationship between the SNR_{sample} and SNR_{integrated} can be derived as in (9).

$$\begin{aligned} \text{var}(D) &= \text{var} \left(\sum_{i=1}^m |c_i - d_i| \right) \\ &= \sum_{i=1}^m \text{var}(|c_i - d_i|) = 2m\sigma^2 \end{aligned} \quad (8)$$

$$\frac{\text{SNR}_{\text{integrated}}}{\text{SNR}_{\text{sample}}} = \frac{m}{2}. \quad (9)$$

REFERENCES

- [1] C. Zierhofer, I. Hochmair-Desoyer, and E. Hochmair, "Electronic design of a cochlear implant for multichannel high-rate pulsatile stimulation strategies," *IEEE Trans. Neural Syst. Rehabil.*, vol. 3, pp. 112–116, Mar. 1995.
- [2] P. Troyk and G. DeMichele, "Inductively-coupled power and data link for neural prostheses using a class-E oscillator and FSK modulation," in *Proc. IEEE 25th EMBS Conf.*, Sep. 2003, vol. 4, pp. 3376–3379.
- [3] W. Liu, K. Vichienchom, M. Clements, S. C. DeMarco, C. Hughes, E. McGucken, M. S. Humayun, E. de Juan, J. D. Weiland, and R. Greenberg, "A neuro-stimulus chip with telemetry unit for retinal prosthetic device," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1487–1497, Oct. 2000.
- [4] M. Ghovanloo and K. Najafi, "A wideband frequency-shift keying wireless link for inductively powered biomedical implants," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 12, pp. 2374–2383, Dec. 2004.
- [5] R. Bashirullah, W. Liu, J. Ying, A. Kendir, M. Sivaprakasam, G. Wang, and B. Pundi, "A smart bi-directional telemetry unit for retinal prosthetic device," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS'03)*, May 2003, vol. 5, pp. 25–28.
- [6] W. Liu and M. S. Humayun, "Retinal prosthesis," in *2004 IEEE ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 218–219.
- [7] W. Liu, M. Sivaprakasam, G. Wang, M. Zhou, J. Granacki, J. Lacoss, and J. Wills, "Implantable biomimetic microelectronic systems design," *IEEE Eng. Med. Biol. Mag.*, vol. 24, pp. 66–74, Sep.–Oct. 2005.
- [8] *IEEE Standard for Safety Levels With Respect to Human Exposure to Radio Frequency Electromagnetic Fields, 3 kHz to 300 GHz* 16, IEEE, Apr. 1999.
- [9] L. Theogarajan, J. Wyatt, J. Rizzo, B. Drohan, M. Markova, S. Kelly, G. Swider, M. Raj, D. Shire, M. Gingerich, J. Lowenstein, and B. Yomtov, "Minimally invasive retinal prosthesis," in *2006 IEEE ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 54–55.
- [10] M. Yuce, "A differential-based multiple bit rate PSK receiver: Theory, architecture, and SOI CMOS implementation," Ph.D. dissertation, Dept. Elect. Eng., North Carolina State Univ., Raleigh, NC, 2004.
- [11] R. G. Vaughan, N. L. Scott, and D. R. White, "The theory of bandpass sampling," *IEEE Trans. Signal Process.*, vol. 39, pp. 1973–1984, Sep. 1991.
- [12] M. Chen, "Power efficient system and A/D converter design for ultra-wideband radio," Ph.D. dissertation, Univ. of California, Berkeley, CA, 2006.
- [13] M. Zhou and W. Liu, "A non-coherent PSK receiver with interference-canceling for transcutaneous neural implants," in *2007 IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 156–157.
- [14] Yukawa, "A CMOS 8-bit high-speed A/D converter IC," *IEEE J. Solid-State Circuits*, vol. 20, no. 6, pp. 775–779, Jun. 1985.
- [15] D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley, 1997.

Mingcui Zhou received the B.S. degree in electrical engineering from Shanghai Jiao Tong University, China, in 2002. She interned at the R&D Department of Alcatel Shanghai Bell in 2002. She received the Ph.D. degree in electrical engineering from the University of California, Santa Cruz, in 2007.

Her research interests are mixed-signal design, integrated circuits for implantable electronics, prosthetic devices, neuroelectronic interfaces, and wireless biotelemetry.

Mehmet Rasit Yuce received the B.S. degree in electronics engineering from Ankara University, Ankara, Turkey, in 1997, the M.S. degree in electrical and computer engineering from the University of Florida, Gainesville, FL, in 2001, and the Ph.D. degree from North Carolina State University (NCSU), Raleigh, NC, in December 2004.

He is currently with the Department of Electrical Engineering and Computer Science, University of Newcastle, Callaghan, NSW, Australia. Between August 2001 and October 2004, he was a research assistant with the Department of Electrical and Computer Engineering at NCSU.

He was a postdoctoral researcher in the Electrical Engineering Department at the University of California at Santa Cruz in 2005. His research interests include analog/digital mixed-signal VLSI for wireless, biomedical, and RF

applications, wireless sensor network for medical monitoring, low-power VLSI circuits for emerging technologies in wireless communications, CMOS transceiver design, and system designs for wireless communications.

Wentai Liu (S'78–M'81–SM'93) received the Ph.D. degree from the University of Michigan, Ann Arbor.

In 1983, he joined North Carolina State University (NCSU), Raleigh, where he held the Alcoa Chair Professorship in the Department of Electrical and Computer Engineering. Since 2003, he has been a Professor in Department of Electrical Engineering, University of California, Santa Cruz, where he is the Campus Director of the NSF Engineering Research Center on Biomimetic Microelectronic Systems.

His research interests include visual prosthesis, implantable electronics, high speed transceiver design (wired and wireless), molecular electronics, microelectronic sensors, timing/clock optimization, on-chip interconnects, and computer vision/image processing. Since its early stages, he has been leading the engineering efforts of the retinal prosthesis to restore vision, finally leading to successful preliminary implant tests in blind patients. He has published more than 150 technical papers and is a coauthor of *Wave Pipelining: Theory and CMOS Implementation* (Kluwer Academic, 1994) and *Emerging Technologies: Designing Low Power Digital Systems* (IEEE Press, 1996).

Dr. Liu has received an IEEE Outstanding Paper Award and the Alcoa Foundation's Distinguished Engineering Research Award.