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Dealing with linear and nonlinear time delays under Model Predictive Control of Power Electronic Inverters

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Abstract—Performance of any digital control scheme applied to inverters, or any other power electronic structures, can significantly suffer due to time delays. These time delays can be linear and nonlinear. An example of a linear delay is the delay due to sampling, control calculation and application of the new voltage state, which results in a constant delay present in each control cycle. An example of a non-linear delay is the inverter dead-time, which is different depending on the selected switching state and the direction of the load current.

Both types of delays are well-known and are addressed in literature. At the same time, the known solutions result in significantly more complicated hardware and/or software implementations. Introduction of MPC to power electronics gives a new and unique opportunity to compensate for both types of the delays in a clear and effective way. This can be done by including the delays, both linear and non-linear, in the model predictions. As an illustration, this paper presents an MPC-based design of closed-loop current control with linear delay compensation for voltage source inverters. The paper also proposes a variable rate MPC-based voltage modulator which combines harmonic suppression with inverter dead-time compensation. The main points of the paper are illustrated by extensive simulation and experimental results.

Index Terms—Model Predictive Control, Delay compensation, Inverter Deadtime, VSI current control.

I. INTRODUCTION AND PROBLEM STATEMENT

Inverters play a central role in modern society including power generation, renewable energy integration, variable speed motor drives in various applications, etc. An inverter is a switching electronic device that generates sinusoidal voltage waveforms, of variable amplitude and frequency, using a DC voltage source as its input. An important issue is that the waveform should be as free as possible from certain types of harmonic distortion for reasons of efficiency, avoiding resonances and electromagnetic interference, as well as for integrity and stability of power infrastructure. However, this problem is made difficult by several core factors especially the inherent switched nature of the waveforms. Also, the switching patterns are perturbed by unavoidable switching delays.

Because of its central importance in the area of switching electronics, the issue of switching delays has been a focus of considerable research attention. We distinguish between control and modulation related switching delays, which are linear, and deadtime related switching delays, which are nonlinear.

A. Linear delays

Control and modulation delays are the result of a finite time taken by a control algorithm to calculate the next inverter state and by a modulator - to apply the calculated state to the inverter output. It is common practice to align

inverter switching with the beginning or/and middle of the control cycle. Consequently, the inverter state calculated at some control cycle will be applied at the beginning of the next control cycle or, at best, the next half cycle [1]. As a result, the entire output waveform of the inverter will be shifted by a constant time interval.

There are well known approaches to compensate for these delays. For example, some researchers [2], [3] propose reducing the control cycle, others [4], [5] propose shifting the control calculations one step back and hence using predicted rather than measured signals. For inverters operating at sampling frequency above 10kHz, control delays are typically neglected [4].

It has been shown in [1], [6] that control and PWM delays is the main factor limiting the bandwidth of the current control loop of a voltage source inverter (VSI), which degrades the reference tracking and disturbance rejection. This is illustrated by simulation results of Fig.1 which show the controlled $\alpha\beta$ -frame currents, the tracking errors and the line currents for a VSI with a proportional resonant (PR) current controller and asymmetrical Space Vector Modulator (SVM) operating at switching frequency of 2100Hz, under a back-emf disturbance condition. Parameters of the PR controller are calculated in accordance with the optimized design recommendations from [1].

In case of Fig.1a the control and modulation delay is zero. The tracking error is minimized by setting the gain of the PR controller to a high value of 25. The resulting performance appears acceptable. In case of Fig.1b a control and modulation delay of one sampling period (or half of SVM cycle) is introduced. Due to a significant reduction of the control bandwidth, the gain of the PR controller had to be reduced to 10, which is the maximum gain for the given stability margin. It is evident from Fig.1b that tracking and disturbance rejection performance of such a controller is very poor.

The problem illustrated in Fig.1 is particularly serious with medium and high voltage inverters which operate at low switching frequencies due to limitations on switching losses. A solution based on state variable feedback proposed in [6], although effective, complicates the current control structure and adds several additional tunable parameters.

In this paper we propose an approach to linear delay compensation which is based on Model Predictive Control (MPC). Under MPC the control and modulation delays can be added to the plant model and included in the model prediction. The generated control action will take the implementation delay into account, and the output current will have no delay relative to the current reference.

(a) No control or PWM delay

(b) Delay of one sampling period

Fig. 1. Performance degradation of current control due to linear delays

B. Nonlinear delays

Deadtime delays is a well-known and very challenging problem in switching electronics. We explain the core concept with the aid of Fig.2. One inverter leg repeatedly shown in Fig.2 includes two switches which states are the inverse of each other at all times except for transitions. To perform a transition, a short time interval is introduced so that complementary switches are not conducting simultaneously. This is done to avoid short circuits across the inverter DC source [7]. This interval is called the inverter deadtime. Its typical duration is between $1\mu\text{sec}$ and $4\mu\text{sec}$. In addition to this deliberately introduced delay, there exist smaller delays related to physical operation of the switches, which we neglect for the sake of simplicity.

An inherent difficulty is that the effect of deadtime on the voltage waveform is dependent upon direction of current in the corresponding inverter leg. In the case illustrated by Fig.2a the current has positive direction $I > 0$ and its path is shown by the red line. Switch SW_A in Fig.2a was initially off (left hand side circuit) and then it switches on (right hand side circuit) via a deadtime state (middle circuit). During the dead time, current is conducted via diode DA , which clamps the output voltage to V^- . The transition from V^- to V^+ thus becomes delayed by the deadtime. A similar situation but with negative current $I < 0$ is shown in Fig.2b. During the deadtime current is conducted by diode DA , which clamps the output voltage to V^+ . As a result, the transition from V^- to V^+ has no delay. The opposite is true for a transition from V^+ to V^- : it is delayed by deadtime if $I < 0$ and has no delay if $I > 0$. Clearly, the deadtime is

Fig. 2. Illustration of deadtime effect on inverter switching (rising edge)

a complex issue.

The essential effect of deadtime is to superimpose an additional series of pulses (bottom plot in Fig.3) on the deadtime-free inverter voltage (top plot in Fig.3). It can be shown that the harmonic spectrum of the deadtime pulses includes low frequency harmonics: odd harmonics for a single phase inverter and $(6n \pm 1)$ harmonics for a three phase inverter. Low frequency harmonics at the inverter output are problematic, and every effort should be taken in the design of switching techniques to avoid them [7]. Despite this effort, low frequency harmonics are usually present at the inverter output due to the deadtime and its companion effects [8].

There have been many suggested approaches to this problem. However, none is accepted as being a comprehensive solution to the issue. Earlier methods ([9], [10]) were primarily hardware based and required integration of elaborate logic circuit into gate control of inverter switchers. More recent approaches have been based around software modifications. A number of papers explored average-value theory, in which the lost volt-seconds averaged over a control cycle are added to the reference voltage according to the direction of the load current [11], [12]. The key challenges of these methods include the correct calculation of the compensation voltage and the accurate detection of the zero current crossing, which are addressed by using specialized current reference frames, ad-hoc adaptive branches, etc. The authors of [13] proposed a pulse-based compensation strategy with calculation of compensated switching times but its accuracy may suffer from subtracting values of close magnitudes.

Fig. 3. Inverter voltage representation: top plot - no deadtime; bottom plot - voltage due to deadtime

Fig. 4. Separation of MPC scheme into a controller and a modulator

All the above techniques are applied to current controlled PWM inverters. There have been limited applications of average volt-seconds adjustment to Direct Torque Controlled inverters (see [14]). The authors of this paper have proposed deadtime compensation within the Model Predictive Control framework [15], which will be discussed further in this paper.

C. Assumptions

1) *Plant model*: Throughout the paper we assume a linear plant model with disturbance given by

$$Ay(z) = Bu(z) + d(z) \quad (1)$$

where $y(z)$ is measured plant output; $u(z)$ is plant input (control); B and A are polynomials of z^{-1} ; and $d(z)$ is disturbance. This assumption agrees with the typical load used with VSI, namely, RL load. For RL load it is true that

$$i(\Delta) = i(0)e^{-\frac{\Delta}{\tau_p}} + \frac{1}{R}V(0)\left(1 - e^{-\frac{\Delta}{\tau_p}}\right) \quad (2)$$

where $i(0)$ and $i(\Delta)$ is current sampled at the beginning and at the end of an interval Δ , respectively; and $\tau_p = L/R$ is the plant time constant; and $V = V(0)$ is constant voltage applied for the entire duration of interval Δ . Model (2) can be further expressed as a discrete model given by:

$$(1 - a_1z^{-1})i(z) = b_1z^{-1}v(z) \quad (3)$$

where $a_1 = e^{-\frac{\Delta}{\tau_p}}$ and $b_1 = \frac{1}{R}\left(1 - e^{-\frac{\Delta}{\tau_p}}\right)$. Moreover, to account for the previously discussed linear (control and modulation) delay, we treat $u(z)$ as the designed control input but the actual voltage applied to the plant is given by $v(z) = z^{-1}u(z)$, so that the following model applies:

$$(1 - a_1z^{-1})i(z) = b_1z^{-2}u(z) \quad (4)$$

One can see that models (3) and (4) fit very well within the assumed class of linear plant models (1). The disturbance included in (1) can be any regular disturbance, such as, back-emf or harmonics.

2) *MPC structure*: We consider standard quadratic cost function for the current error, which is typically used in horizon 1 MPC for VSI and is given by:

$$J_k = \left(i_\alpha^*(k) - \hat{i}_\alpha(k+1)\right)^2 + \left(i_\beta^*(k) - \hat{i}_\beta(k+1)\right)^2 \quad (5)$$

where i^* denotes reference and $\hat{i}$ denotes predicted values of the current components in $\alpha\beta$ frame.

It has been previously shown by the authors ([16], [17]) that, by transferring the cost function (5) to voltage domain, it is possible to represent the finite set (FS) horizon 1 MPC as a combination of two components: inversion of the plant model (3) and a nearest neighbour

quantizer, which selects an available voltage from the finite set as close as possible to the desired voltage. Such an interpretation of MPC is shown schematically in Fig.4a.

An important consequence of this interpretation is the separation of the controller part and the modulator part of the MPC scheme. This opens a door for various performance improvements of the MPC scheme, including:

- Modification of the modulator part and turning the nearest neighbour quantizer into a feedback quantizer shown in Fig.4b. Note that with the feedback filter $H(z) = z^{-1}$ the modulator in Fig.4b is equivalent to the nearest neighbour quantizer. By an appropriate design of the feedback filter $H(z)$ it is possible to achieve improved tracking at the fundamental frequency and/or rejection of a single or multiple harmonic components. This is discussed in detail in [18], [19].
- Alternatively, replacement of the modulator part with a standard PWM or SVM, which is equivalent to replacement of a finite control set in the MPC scheme with a convex control set.
- Modification of the controller part to achieve improved reference tracking and disturbance rejection. One possible version of the improved controller is shown in Fig.4b as an anti-windup PI controller. In [16], [20] it has been shown that such a controller is indeed the optimal controller, which minimizes the cost function (5) for a model given by (1) without an additional control delay as per (3) and with a constant disturbance $d = d_0$.

The above modifications broaden the interpretation of MPC. It suggests that, provided that the controller is designed based on model prediction and cost function minimization, it is inherently MPC, regardless of the type of modulator being used: finite control set or convex control set. Such an interpretation contributes to the ongoing research into MPC-based PWM-like modulation schemes with constant switching frequency [21], [22].

With this understanding, we will illustrate different points on different versions of MPC. In chapter 2 compensation of linear delays will be illustrated using an MPC-based controller and an SVM modulator. The type of modulator is not relevant in this case, but with an SVM or PWM modulator linear delays (corresponding to a PWM cycle) are typically a much bigger issue than with a finite set modulator. The finite set modulator selects only one switching state over its cycle and typically operates at a much faster sampling frequency than SVM or PWM.

In chapter 3 compensation of nonlinear (deadtime) delays will be illustrated using a finite set modulator (specifically, a feedback quantizer) with suppression of

multiple harmonic components. Again, similar approach can be applied to any other modulator, but for a feedback quantizer the deadtime compensation is particular critical.

In conclusions, this paper will summarise the proposed methods of linear and non-linear delay compensation methods for power electronic inverters. It should be noted that, since early introduction of MPC to power electronics a question has been asked: “does MPC really do anything that traditional approaches cannot do as well if not better?” It is the opinion of the authors of this paper that delay compensation is indeed a case where MPC thinking leads to a novel solution that would otherwise be difficult to conceive from traditional viewpoints.

II. COMPENSATION OF LINEAR DELAYS IN MPC FRAMEWORK

In this section we start with presenting a general approach in a form of a step-by-step procedure. We then develop current controllers with linear delay compensation for two important cases: tracking of a constant reference in the presence of a constant disturbance and tracking of a harmonic reference in the presence of a harmonic disturbance.

A. General approach

1) We assume the plant model (1) which has a two-step delay (as in (4)): one from the plant itself and one due to the control/modulator. This means that the lowest power of A is z^0 and the lowest power of B is z^{-2} . Also we assume that $a_0 = 1$, which can be always achieved by dividing both A and B by a constant.

2) We can further express the measured output in terms of reference $y^*(z)$ and tracking error $e(z)$ as: $y(z) = y^*(z) + e(z)$

3) Say that disturbance model has a nulling operator D_1 such that $D_1 d(z) = 0$ where D_1 is polynomial of z^{-1} . Similarly, reference signal has a nulling operator D_2 such that $D_2 y^*(z) = 0$ where D_2 is polynomial of z^{-1} . Then, multiplying both sides of (1) by $D = D_1 D_2$ yields

$$ADe(z) = BDu(z) \quad (6)$$

Note that, in some cases, $D_1 = D_2$. This is true, for example, when tracking a constant reference in the presence of a constant disturbance, or tracking a sinusoidal reference in the presence of a sinusoidal disturbance. In such cases we only use one nulling operator, i.e. $D = D_1 = D_2$. For the sake of space, notation “(z)” will be omitted hereafter.

4) We divide both sides of (6) by a polynomial C which is one order lower than the maximum power of z^{-1} in AD and $c_0 = 1$ for simplicity:

$$\frac{AD}{C}e = \frac{BD}{C}u \quad (7)$$

5) We factor transfer function $\frac{AD}{C} = 1 - \frac{C-AD}{C}$. As a result, the lowest power of $(C-AD)$ is z^{-1} . By choosing an appropriate coefficient c_1 we cancel the z^{-1} term. Now the lowest power of $(C-AD)$ is z^{-2} . The lowest power of (BD) is also z^{-2} . Then (7) transforms into:

$$e = \frac{C-AD}{C}e + \frac{BD}{C}u \quad (8)$$

6) Note that the right hand side of expression (8) depends only on past values of e and u . The left hand side of (8) is the most recent value of e . Now we advance both sides of (8) by two steps, forming a two-step ahead prediction $z^2 \hat{e}$ (corresponding to $\hat{e}(k+2)$).

$$z^2 \hat{e} = \frac{z^2(C-AD)}{C}e + \frac{z^2 BD}{C}u \quad (9)$$

7) Now the lowest power of both $z^2(C-AD)$ and $z^2 BD$ in the right hand side of (9) is z^0 . We factor transfer function as $\frac{z^2 BD}{C} = b_1 - \frac{b_1 C - z^2 BD}{C}$, which yields:

$$z^2 \hat{e} = \frac{z^2(C-AD)}{C}e + b_1 u - \frac{b_1 C - z^2 BD}{C}u \quad (10)$$

8) We apply a quadratic cost function to the tracking error as:

$$J = [\hat{e}(k+2)]^2 \quad (11)$$

Clearly cost function (11) will be minimized if $\hat{e}(k+2) = 0$. Note that the last term in (10) depends only on the past values of u which cannot be changed but are known. The only control value that can be used to minimize the cost function (11) is $b_1 u(z)$, i.e the most recent (new) control value. We express $b_1 u(z)$ by rearranging (10) and then divide both sides by b_1 , which gives the optimal control u^{opt} in the sense of the cost function (11):

$$u^{opt} = \frac{1}{b_1} \left\{ \frac{b_1 C - z^2 BD}{C}u - \frac{z^2(C-AD)}{C}e \right\} \quad (12)$$

9) Expression (12) corresponds to the unconstrained optimal control law. If u^{opt} is outside the constraint boundary then we find constrained control law $u_{con}^{opt}(k)$ which is as close as possible to the unconstrained $u^{opt}(k)$ (i.e. lies on the constraint boundary).

B. Time delay compensation for a model with constant reference and disturbance

It is common in power electronics applications to track sinusoidal references. However, when control is performed in a synchronously rotating reference frame then the reference and all disturbances at fundamental frequency are seen as being constants, hence a PI current controller is typically used [1]. The disturbances include, for instance, current cross-coupling terms or back-emf disturbances.

Fig. 5. Optimal PI controller with control delay compensation

Fig. 6. Pole-zero maps for optimal controllers including control delay compensation

We modify the model (4) into the following form, including disturbance:

$$(1 - a_1^2 z^{-2}) (e + i^*) = b_1 z^{-2} (1 + a_1 z^{-1}) u + d \quad (13)$$

The common nulling operator of both reference and disturbance is $D(z) = 1 - z^{-1}$, which can be easily checked by: $d(k) - d(k-1) = d_0 - d_0 = 0$. The C polynomial has the form: $C(z) = 1 + c_1 z^{-1} + c_2 z^{-2}$. Then

$$\begin{aligned} & \frac{(1 - a_1^2 z^{-2}) (1 - z^{-1})}{1 + c_1 z^{-1} + c_2 z^{-2}} e \\ &= b_1 z^{-2} \frac{(1 + a_1 z^{-1}) (1 - z^{-1})}{1 + c_1 z^{-1} + c_2 z^{-2}} u \end{aligned} \quad (14)$$

We use $c_1 = -1$ and $c_2 = \varepsilon$. Following the steps (8) to (12), we obtain the unconstrained optimal control law as:

$$\begin{aligned} u^{opt} &= \frac{1}{b_1} \frac{a_1^2 (1 - z^{-1}) + \varepsilon}{1 - z^{-1} + \varepsilon z^{-2}} (i^* - i) \\ &- \frac{a_1 z^{-1} (1 - z^{-1}) - \varepsilon z^{-2}}{1 - z^{-1} + \varepsilon z^{-2}} u \end{aligned} \quad (15)$$

Finally, we find constrained control law $u_{con}^{opt}(k)$ which is as close as possible to the unconstrained $u^{opt}(k)$ given by (15). Note that MPC approach automatically resulted in an anti-windup form of the optimal controller. To understand the nature of the optimal controller with delay compensation, we convert the control law into conventional form as:

$$C_{PI}^d(z) = \frac{1}{b_1} \frac{a_1^2 (1 - z^{-1}) + \varepsilon}{(1 + a_1 z^{-1}) (1 - z^{-1})} \quad (16)$$

Fig.6a shows a pole-zero map for the optimal controller (16), which is very similar to that of a PI controller. In addition to a pole at $z = 1$ and a nearby zero, which is typical for a PI controller, one can see a negative pole at $z = -a_1$ and a zero close to the origin, which originated from the additional delay in the plant model. We call this new structure a “modified PI controller”.

We can calculate sensitivity S , which determines disturbance rejection, and complementary sensitivity T , which determines reference tracking, as follows:

$$S = \frac{(1 - a_1^2 z^{-2}) (1 - z^{-1})}{1 - z^{-1} + \varepsilon z^{-2}} \quad (17)$$

$$T = \frac{z^{-2} [a_1^2 (1 - z^{-1}) + \varepsilon]}{1 - z^{-1} + \varepsilon z^{-2}} \quad (18)$$

One can easily check that $S = 0$ and $T = 1$ at three frequencies, namely, when $z = \pm a_1$ and $z = 1$. Therefore, any constant reference is perfectly tracked and any constant disturbance is perfectly rejected.

Figs.5a and 5b show block diagrams of the optimal controller described by (16) and (15), which are the conventional and the anti-windup forms of the same controller, respectively.

To address the PWM delay issue, it was previously proposed in [1] to use a conventional PI controller with a modified time constant. In this paper we have shown that the optimal performance of the system with PWM delay will be achieved by modifying the entire structure of the conventional PI controller into the scheme shown in Fig.5.

C. Model with sinusoidal reference and disturbance at fundamental frequency

If VSI current control is performed in a stationary reference frame then both the reference and the major disturbances (current cross-coupling and back-emf) are seen as sinusoidal signals at fundamental frequency. In such applications it is common to use a PR controller for VSI current control [1].

To compensate for the control/modulo delay, we use the same plant model as in (13) except that we use a harmonic disturbance at frequency ω_0 given by: $d(k) = O_1 \cos(\omega_0 \Delta k + \varphi)$. The nulling operator for both single frequency reference and single frequency disturbance is given by $D(z) = 1 - 2 \cos(\omega_0 \Delta) z^{-1} + z^{-2}$. This can be easily confirmed by showing that: $\cos(\omega_0 \Delta k + \varphi) + \cos(\omega_0 \Delta(k+2) + \varphi) = 2 \cos(\omega_0 \Delta) \cos(\omega_0 \Delta(k+1) + \varphi)$.

The C polynomial has the form: $C(z) = 1 + c_1 z^{-1} + c_2 z^{-2} + c_3 z^{-3}$. We use $c_1 = -2 \cos(\omega_0 \Delta)$, $c_2 = 1 + \varepsilon$ and $c_3 = -\varepsilon$ to simplify the control law. Following the steps (8) to (12), the unconstrained optimal control law results:

$$\begin{aligned} u^{opt} &= (i^* - i) \times \\ & \frac{1}{b_1} \frac{a_1^2 + \varepsilon - (2a_1^2 \cos(\omega_0 \Delta) + \varepsilon) z^{-1} + a_1^2 z^{-2}}{1 - 2 \cos(\omega_0 \Delta) z^{-1} + (1 + \varepsilon) z^{-2} - \varepsilon z^{-3}} - \\ & \frac{a_1 z^{-1} - (2 \cos(\omega_0 \Delta) + \varepsilon) z^{-2} + (a_1 + \varepsilon) z^{-3}}{1 - 2 \cos(\omega_0 \Delta) z^{-1} + (1 + \varepsilon) z^{-2} - \varepsilon z^{-3}} u \end{aligned} \quad (19)$$

Converting of the control law (19) into conventional form yields a “modified PR controller” given by:

$$C_{PR}^d(z) = \frac{1}{b_1} \frac{a_1^2 (1 - 2 \cos(\omega_0 \Delta) z^{-1} + z^{-2}) + \varepsilon (1 - z^{-1})}{(1 + a_1 z^{-1}) (1 - 2 \cos(\omega_0 \Delta) z^{-1} + z^{-2})} \quad (20)$$

Fig. 7. Optimal PR controller with control delay compensation. Note: $L(z) = 1 - 2 \cos(\omega_0 \Delta) z^{-1} + z^{-2}$

Fig. 8. Current control with and without linear delay compensation

Fig.6b shows a pole-zero map for the optimal controller (20). In addition to a pair of poles at $z = e^{\pm j\omega_o\Delta}$ and nearby zeros, as expected from a PR controller, one can see a negative pole at $z = -a_1$ and a zero close to the origin, which originate from the additional delay in the plant model. We can also calculate sensitivity and complementary sensitivity functions and check that $S = 0$ and $T = 1$ at four frequencies, namely, when $z = \pm a_1$ and $z = e^{\pm j\omega_o}$. Therefore, a harmonic reference at frequency ω_o is perfectly tracked and any disturbance at the same frequency is perfectly rejected.

Fig.7a and 7b show block diagrams of the optimal controller described by (20) and (19), which are the conventional and the anti-windup forms of the same controller, respectively. Simulation results illustrating performance of a standard PR current controller and of an optimal PR current controller designed in accordance with (19), are shown in Figs.8a and 8b, respectively. These results were obtained in the presence of back-emf disturbance equal to half the maximum output voltage of the inverter. Fig.8b shows practically no current error at fundamental frequency as expected.

We again note that for systems with PWM delay it was previously proposed in [1] to use a conventional PR controller with a modified time constant. In this paper we have shown that the optimal performance of the system with PWM delay will be achieved by modifying the entire structure of a conventional PR controller into the scheme shown in Fig.7. For experimental results illustrating performance of optimal current controllers designed in MPC framework to compensate for linear delays, the reader can be referred to [20].

III. DEADTIME COMPENSATION IN MPC FRAMEWORK

As discussed in chapter 1, the use of MPC for deadtime compensation will be illustrated on a case where this compensation is particularly critical and its effect is very obvious. The authors have previously proposed harmonic suppression scheme [18], [19] based on the use of feedback quantizer (FBQ) modulator as shown in Fig.4b and repeated in Fig.9a. The core idea was to design the transfer function $(1 - H(z))$ so that it had nulls at the frequencies where harmonic suppression was sought. This is achieved

by a special design of the feedback filter $H(z)$ as discussed in [18]. Fig.10a shows the magnitude of the voltage and current spectra in the absence of switching delays. We see from Fig.10a that the circuit indeed achieves excellent harmonic suppression at the 3rd, 5th and 7th harmonics as required by the design.

However, when minor ($5\mu s$) deadtime delays were introduced, the result changes to that shown in Fig.10b. Clearly, the small nonlinear delays have destroyed the excellent result shown in Fig.10a. Instead of the harmonic suppression expected from the feedback filter, one observes spectral peaks at the 3rd, 5th and 7th harmonics!

To develop the deadtime compensation strategy we use the earlier established fact that the FBQ circuit shown in Fig.9a implements the cost function minimization part of the horizon 1 MPC. It minimizes the distance (or norm) between the selected state v and the internal variable v_d . By using a simple algebra it can be shown that

$$v_d = v^* - Hv + Hv_d \quad (21)$$

which is equivalent to

$$v_d - v = \frac{1}{1 - H(z)} (v^* - v) = F(z) (v^* - v) \quad (22)$$

Therefore, by minimizing the norm $\|v_d - v\|$, the FBQ circuit actually minimizes the voltage error passed through the filter $F(z) = \frac{1}{1 - H(z)}$. The purpose of the filter $F(z)$ is to define weightings applied to different spectral components of the voltage error. This explains how FBQ achieves harmonic suppression of the selected frequencies. Moreover, this understanding helps developing a path for the deadtime compensation.

Since the objective is to minimize the filtered voltage error, we can calculate such a filtered error for all candidate states. Depending on current direction, some states may have an associated deadtime delay and some may have no deadtime delay. For example, the candidate state V_j in Fig.9b would result in immediate switching, while the candidate state V_k in Fig.9c would have a switching delay. These details are included in estimation of the corresponding cost functions $E_j(\Delta)$ and $E_k(\Delta)$, which are calculated as the filtered voltage error at the end of the control interval Δ .

Fig. 9. Illustration of deadtime compensation using variable horizon MPC

Fig. 10. Effects of dead time and its proposed compensation on harmonic spectrum of voltage and current

To perform the above calculation and account for deadtime delays, the filter output has to be calculated at a much faster rate than the sampling rate Δ . With relation to Fig.9c, the sampling interval of the digital filtering has to be at least as small as the deadtime delay Δ_1 . Such a fast filtering implementation would be very demanding in terms of computational resources.

However, in practical situations where MPC is typically performed with a constant sampling interval Δ , there exist only a very limited number of different intervals over which the voltage state remains constant. With relation to Fig.9 there are only three such intervals, namely Δ , Δ_1 and $1 - \Delta_1$. For these sampling intervals three different designs of the digital filter $F(z) = \frac{1}{1-H}$ can be implemented, denoted as $F^\Delta(z)$, $F^{\Delta_1}(z)$ and $F^{1-\Delta_1}(z)$. Therefore, to calculate $E_j(\Delta)$ it will be necessary to pass one sample of $(v^* - V_j)$ through the filter $F^\Delta(z)$, and to calculate $E_k(\Delta)$ - to pass one sample of $(v^* - V_k)$ through the filter $F^{\Delta_1}(z)$ and to pass another sample of $(v^* - V_k)$ through the filter $F^{1-\Delta_1}(z)$. Such a calculation

is, at most, twice as long as the FBQ implementation without deadtime compensation, which looks like a fair price giving the resulting performance improvement.

The results are illustrated in Fig.10c where the same $5\mu s$ deadtime delay was applied as in the case of Fig.10b but this delay was accounted for in the MPC algorithm. Fig.10d combines the three plots for the ease of comparison. It is evident from Fig.10d that the modified MPC with deadtime compensation performs as well as the original MPC in the absence of deadtime delays.

It can be noted that 1 or 2% errors were important when implementing the resonant filter $H(z)$. In particular, we have used parallel second order sections implemented in delta domain. Thus we deployed state of the art ideas in numerical aspects of sampled data system theory (see [23], [24]) to achieve these results. The variable rate MPC algorithm was successfully implemented in laboratory on a TMS320F28335 processor at 5kHz sampling rate. Experimentally obtained spectrum of line-to-line voltage is shown in Fig.11. In this experiment harmonic suppression

Fig. 11. Experimental results for deadtime compensation

is achieved at 5th, 7th, 11th, 13th and 17th harmonics of the fundamental frequency, along with deadtime compensation using the described variable rate MPC algorithm.

IV. CONCLUSIONS

The paper has discussed linear and nonlinear delays in power electronic inverters, the effects of these delays on the performance of VSI current control, and the existing mitigation and compensation methods.

The paper has proposed methods for compensation of such delays based on using MPC framework.

It suggested that linear (control and modulator related) delays are better compensated in the current control design and presented a general approach as well as two important practical examples of MPC-based current control design with inclusion of linear delays in the plant model. The paper demonstrated that linear delays are completely eliminated by such a design, resulting in improved reference tracking and disturbance rejection.

The paper also suggested that nonlinear (deadtime related) delays can be compensated in the modulator part of the MPC scheme by inclusion of such state-dependent delays in the cost function estimation. It has proposed a variable rate MPC algorithm as a practical way to implement the deadtime compensation without a significant computational burden.

The proposed approaches to the linear and nonlinear delay compensation are independent of each other and can be applied separately or in combination with each other.

The methods of delay compensation presented in the paper have been illustrated by simulation and experimental results.

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