Comparison of Three Harmonic Extraction Techniques for Active Filters

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Abstract—Active filter relies heavily on the extraction of the harmonics to be eliminated from the supply waveforms. There are a variety of techniques available for achieving this. These techniques range from bandpass filters, to various configurations of phase locked loops, or synchronous rotating frame transformations and low pass filtering. This paper will introduce a variant of the standard PLL structure called the Advanced PLL, and then compare its performance against two other published PLL based techniques for harmonic extraction.

I. INTRODUCTION

In active filter applications the required harmonics to be eliminated in the voltage or current waveforms have to be identified. If selective harmonic cancellation is required, the most obvious technique is to use a conventional digital band-pass filter. The pass-band of such a filter has to be very narrow because the frequency separation between harmonics is often only small (e.g. such as when filtering the 5th and 7th harmonics).

Ideally the phase shift from a band pass filter is zero if the harmonic frequency is at the centre of the filter pass band. However, if it isn’t, then the phase shift can be large due to the very rapid phase change around the centre frequency. The supply frequency can be different from the assumed supply frequency due to system load changes or fault conditions. It is possible to make the supply frequency different from the assumed supply frequency, for example, by using a PLL. The PLL has to use integral phase feedback so that there is no steady state phase error between the estimated and actual phase.

Remark 1: The PLL has to use integral phase feedback so that there is no steady state phase error between the estimated and actual phase.

A. Synchronous frame harmonic extraction

A common approach for harmonic extraction uses three phase synchronous modulation/demodulation [2]–[4]. The basic idea is shown in Fig. 1. Notice that a PLL is used to generate the supply frequency, angle and phase locked waveforms.

The remainder of this paper will discuss three different techniques for extracting harmonics using PLLs. The algorithms will be briefly discussed and their performance compared via simulation for extracting the fundamental, 5th and 7th harmonics.

1Note that the 5th harmonic is a negative sequence, hence the negative sign on the rotation direction.
Waveform

Feedback control

Input

LPF and PI feedback

Phase detector

VCO

Figure 1: Akagi active filter control and harmonic extraction technique

Figure 2: Karimi-Ghartemani EPLL block diagram.

Fig. 1 shows the Akagi control approach for an active filter (including the capacitor DC voltage control for the inverter) [3]. However, the relevant section with respect to this paper is the extraction of the 5th harmonic using the dq transformations together with high and low pass filters in both the feedback and feed-forward loops respectively. The crucial part relevant to this paper is the generation of the feed-forward harmonic reference currents.

B. Enhanced Phase Locked Loop

Another PLL technique was developed by Karimi-Ghartemani [5]–[9]. This is known as the Enhanced PLL (EPLL). His approach is interesting in that it uses single phase PLLs with a complex non-linear feedback that is able to accurately estimate not only the phase of the input waveform, but also its amplitude. Karimi-Ghartemani has published a non-linear stability analysis of the EPLL and has shown that it is stable (although from the authors simulations it appears to go unstable when high gains are couple with large input signals) [5]. The basic structure of this algorithm appears in Fig. 2. The main difference between the EPLL and other published PLLs is in the phase detector part of the circuit which includes feedback that estimates the amplitude (A) of the sinusoidal component of the incoming waveform that is close to the centre frequency \( \omega_c \). The PI feedback in the phase error loop means that the EPLL achieves zero phase error.

Remark 2: Two points to note about the EPLL: (i) it can be implemented in analogue or digital form. The digital version contains multiply functions, and computationally mirrors the analogue version; (ii) the low pass filters in the loop are optional and are suggested by Karimi-Ghartemani to improve the performance of the loop in the presence of noise. ■

When used for harmonic filtering EPLLs are cascaded with the error signal \( e \) being fed from one EPLL to the next as shown in Fig. 3. As one proceeds down the EPLL chain the signal fed into the next EPLL only has the harmonics present corresponding to the order of the EPLL and above. Karimi-Ghartemani suggests that the signals fed into the various EPLLs can be scaled in amplitude based on the harmonic order to improve performance [7].

C. Advanced Phase Locked Loop

A third approach, proposed by the authors, uses a slightly different PLL structure which will be called an Advanced PLL (APLL). Fig. 4 shows its structure. This particular diagram shows two APLLs configured together, one to identify the fundamental and the other the 5th harmonic. If more harmonics are required then extra APLLs can be similarly configured.

There are several significant differences between the APLL and the EPLL, namely:

- The APLL is a three phase PLL, whereas the EPLL is a single phase.
- The phase comparator uses a pure phase error calculation and therefore the feedback phase error is a DC value once locked.
- The amplitude is detected using a non-feedback process. This averts possible stability problems associated with feedback on the amplitude.
- The individual APLLs have the output from all the other APLLs subtracted from their input waveform prior to processing.

The phase error for the APLL is determined from the two phase equivalent waveforms, unlike other three phase PLLs that use a \( d \) axis subtraction [10], which is equal for the phase error for small errors. Due to the sign change properties of the cosine function that is implicitly associated with the \( d \) axis calculation this approach may have problems under high phase error conditions.
II. SIMULATION RESULTS

In order to test the above algorithms a digital simulation was written. The low pass filters used in all the simulations are 1st order. The basic waveform used to test the PLLs is of the form:

\[
\begin{align*}
    x_a &= 100 \sin(\omega t + k_1 \delta_1) + 30 \sin(5\omega t + k_5 \delta_5) \\
    &\quad + 15 \sin(7\omega t + k_7 \delta_7) \\
    x_b &= 100 \sin(\omega t - \frac{2\pi}{3} - k_1 \delta_1) \\
    &\quad + 30 \sin \left[5(\omega t - \frac{2\pi}{3}) - k_5 \delta_5 \right] \\
    &\quad + 15 \sin \left[7(\omega t - \frac{2\pi}{3}) - k_7 \delta_7 \right] \\
    x_c &= 100 \sin(\omega t + \frac{2\pi}{3} - k_1 \delta_1) \\
    &\quad + 30 \sin \left[5(\omega t + \frac{2\pi}{3}) - k_5 \delta_5 \right] \\
    &\quad + 15 \sin \left[7(\omega t + \frac{2\pi}{3}) - k_7 \delta_7 \right]
\end{align*}
\]

where \(\omega = 307.88\) rads/sec (49 Hz supply frequency\(^2\)). The PLLs in the simulation assume that the supply frequency is 50 Hz. The simulation allows the basic waveforms to be modified with large amplitude glitches, and harmonic amplitude and phase variations. This is to test the tracking of the three schemes under such conditions. The glitch in the input waveform multiplies the composite waveform amplitude by 5, and the glitch is there for 10 samples (i.e. 2msec). There is an step amplitude change at the mid point (5000 samples) into the simulation. Only the amplitude of the harmonics have been changed by multiplying the 5th and 7th harmonics by 1.3 and 1.4 respectively. This is designed to test the performance of the fundamental harmonic estimation with respect to changes in the amplitudes of other harmonics, and also the transient harmonic amplitude estimation performance. The last transient input is a harmonic phase change. This is a relative phase change between the fundamental and its harmonics. The initial phase shift of the 5th harmonic is \(\delta_5 = \frac{\pi}{3}\) rads, and the 7th harmonic \(\delta_7 = \frac{\pi}{2}\) rads (note \(\delta_1 = 0\)). These initial phase offsets are then multiplied by \(k_5 = 2.0\) and \(k_7 = 2.5\) respectively at 8000 samples.

Remark 3: The above waveforms were chosen so that certain real conditions could be represented. Regardless of the validity of the simulated conditions, the relative performance of the algorithms is still a valid measure.

Fig. 5 shows a portion of the input waveform at the point of the glitch. The \(x\) axis is sampling points, with each sample being 200\(\mu\)sec apart (5kHz sampling). The first set of results are generated for the situation where the VCO centre frequencies of the various cascaded PLL, APLL and EPLL modules are set to \(n\omega_0\) where \(\omega_0 = 50\) Hz and \(n\) is the harmonic order.

Fig. 6 shows the error between the estimated fundamental and the true fundamental for the APLL, EPLL and Synchronous Demodulation (SyncDemod) algorithms. The glitch that occurs in the input at the 3000 sample point causes both the APLL and EPLL loops to deviate substantially, but they are able to re-lock to the fundamental after approximately 0.1 sec (i.e. 5 mains cycles). The synchronous demodulation technique shows very little error due to this glitch. The reason for this can be seen from the very slow convergence rate of this technique caused by the very low pass filters used.
The PLL based techniques have excellent rejection properties with respect to harmonic amplitude transients – the transient present at the 5000 sample point can hardly be seen in the fundamental error for these strategies. The SyncDemod technique on the other hand does allow some of the harmonic amplitude changes to seep through into the fundamental estimate. The other observation that can be made from Fig. 6 is that the performance of the APLL is excellent when there are no disturbances. One can see that there is almost no ripple in the error for this strategy, whereas both the EPLL and the SyncDemod techniques have a small output ripple.

Remark 4: The excellent steady state performance of the APLL is obtained at the cost of a slightly worse disturbance rejection performance compared to the EPLL and SyncDemod. The reason for both of these effects is the multiple feedback loops in the APLL structure.

Similarly Fig. 7 shows the error in the 5th and 7th harmonics for the three different approaches. The performance of the APLL under the condition of an erroneous assumed frequency is clearly much superior to the other strategies. In fact, the other strategies have unacceptable performance. The transient performance of the SyncDemod approach is also very slow. If one increases the bandwidth of the filters to improve the transient response, then the feed-through of undesirable frequencies increases even further.

The final set of results are for the situation where there is no error between the assumed fundamental frequency of the waveform and the true fundamental frequency. We shall only consider the performance of the harmonic estimation under this scenario, since the fundamental estimation performance is very similar for all the approaches. The plots for this appear in Fig. 8. As can be seen, under this condition the APLL approach is still clearly superior to the EPLL and SyncDemod techniques, however the performance of the two PLL techniques are both much better than the SyncDemod approach. The gains used in the feedback loops of the PLLs are the same as those used in the previous case.

III. CONCLUSION

This paper has compared the performance of three harmonic extraction techniques suitable for use in power electronic applications – the APLL, the EPLL, and a synchronous demodulation technique. The APLL uses a multiple harmonic feedback approach and an ideal phase comparator that gives it performance advantages compared to the other two techniques. The authors have also successfully used of the APLL for the extraction of positive and negative sequences. This is the subject of a future paper.

REFERENCES


Figure 7: 5th harmonic and 7th harmonic errors for the APLL, EPLL and Synchronous Demodulation. Supply frequency = 49Hz, VCO frequency = 50 Hz.


Figure 8: 5th and 7th harmonic errors for the APLL, EPLL and Synchronous Demodulation. Supply frequency = VCO frequency = 50 Hz.